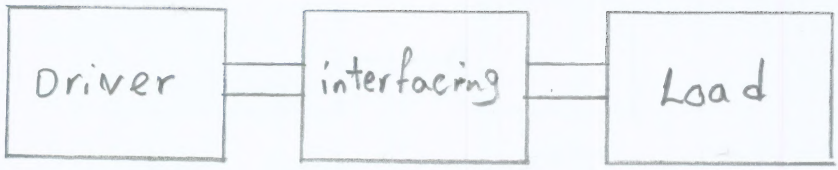
Digital Lec (4) 19/10/2016

Interfaceing CMOS & TTL families

Ref:

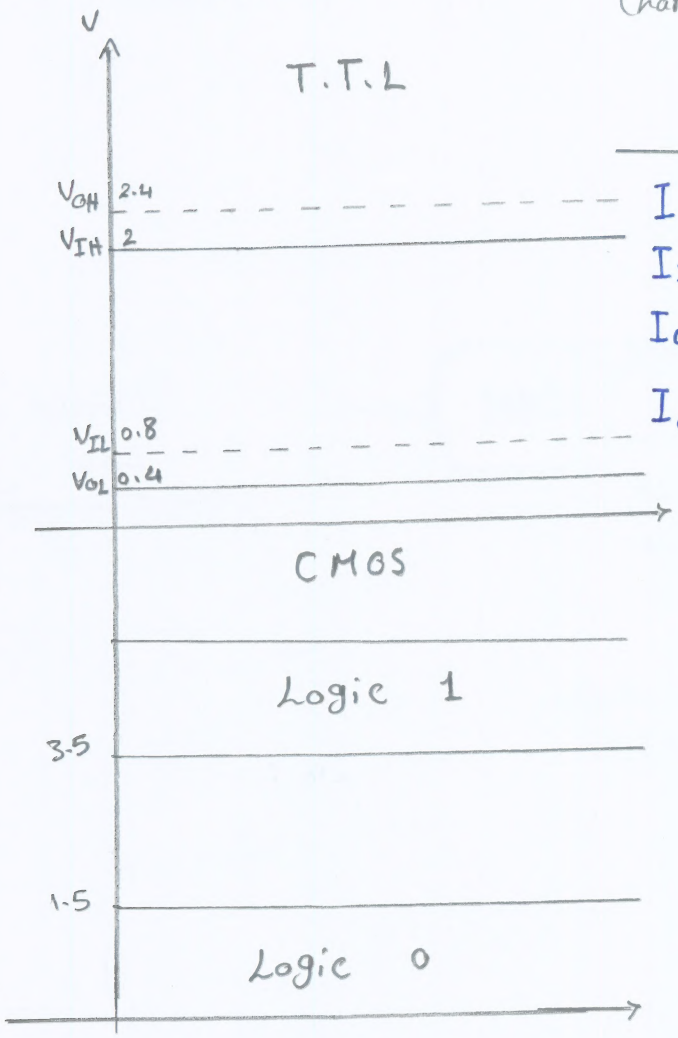
o/p current

o/p voltage



Charactrestic

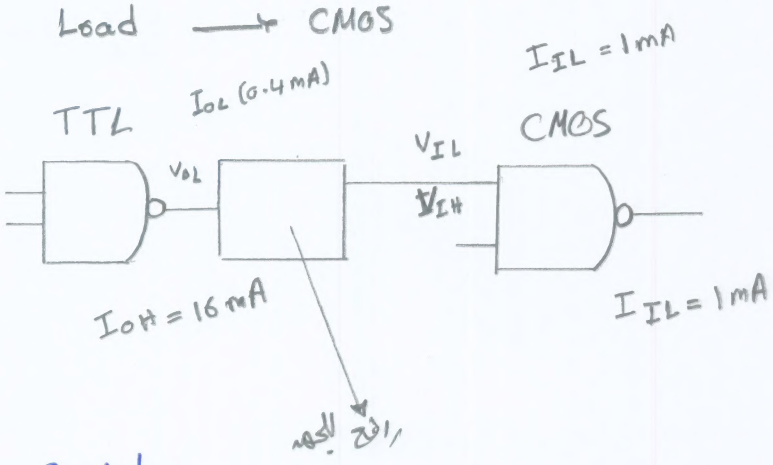
Charactrestic



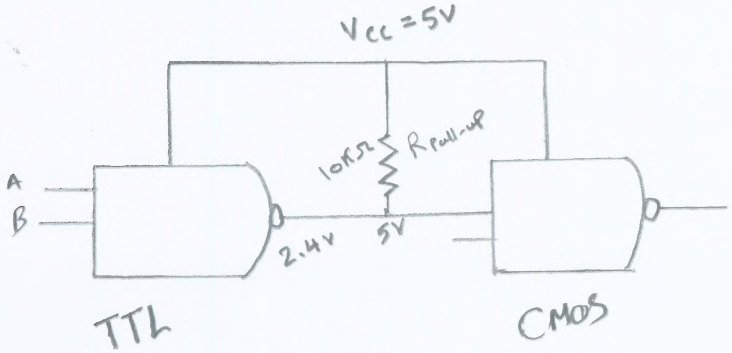
	CMOS 4000	CMOS 74CXX	(TTL) 74 XX
I_{IH}	1 mA	1 mA	40 mA
I_{IL}	1 mA	1 mA	1.6 mA
I_{OL}	0.4 mA	4 mA	16 mA
I_{OH}	0.4 mA	4 mA	0.4 mA

driver ⟶ TTL

Load ⟶ CMOS



Pull-up Resistor

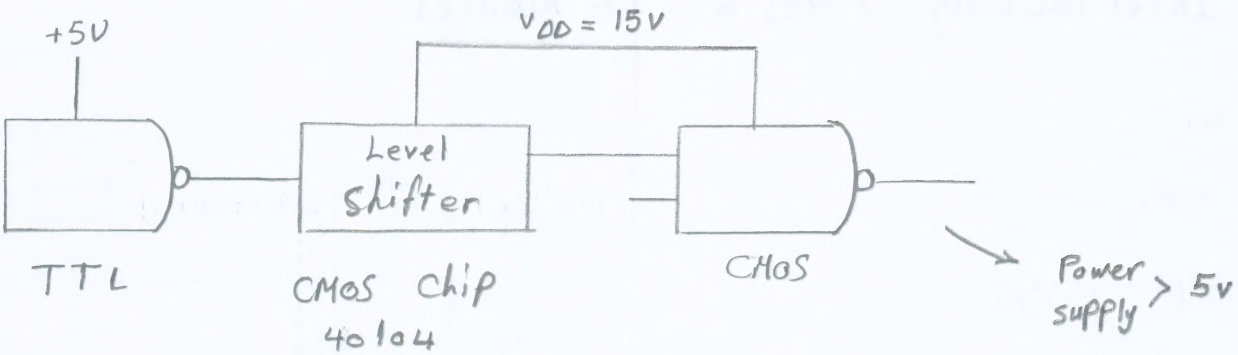


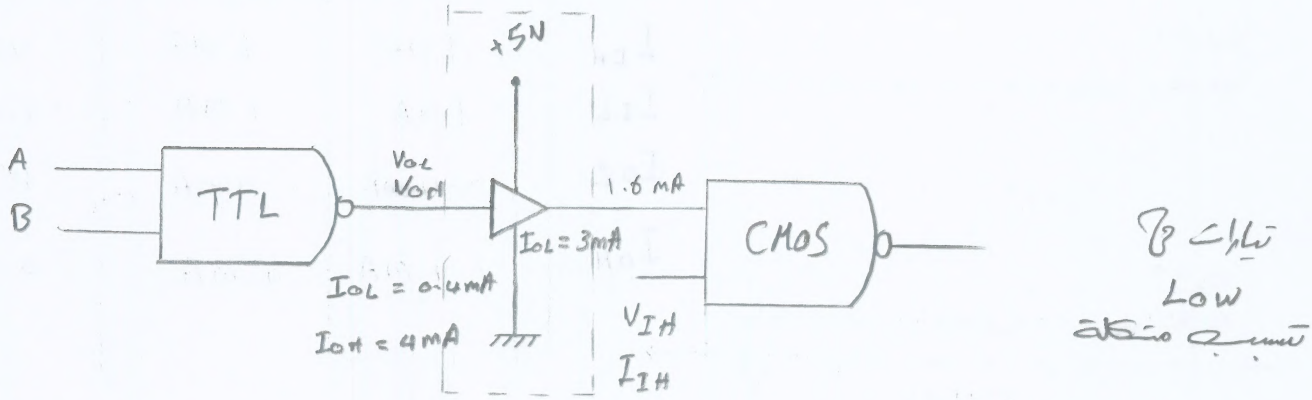
Power supply 5V

TTL → 5V (Power supply)

CMOS → 3.15V (Power supply)

TTL driver for High voltage of CMOS (3 → 15 V)





I_{OL} = 3mA

Emitter Coupled Logic (E.C.L)

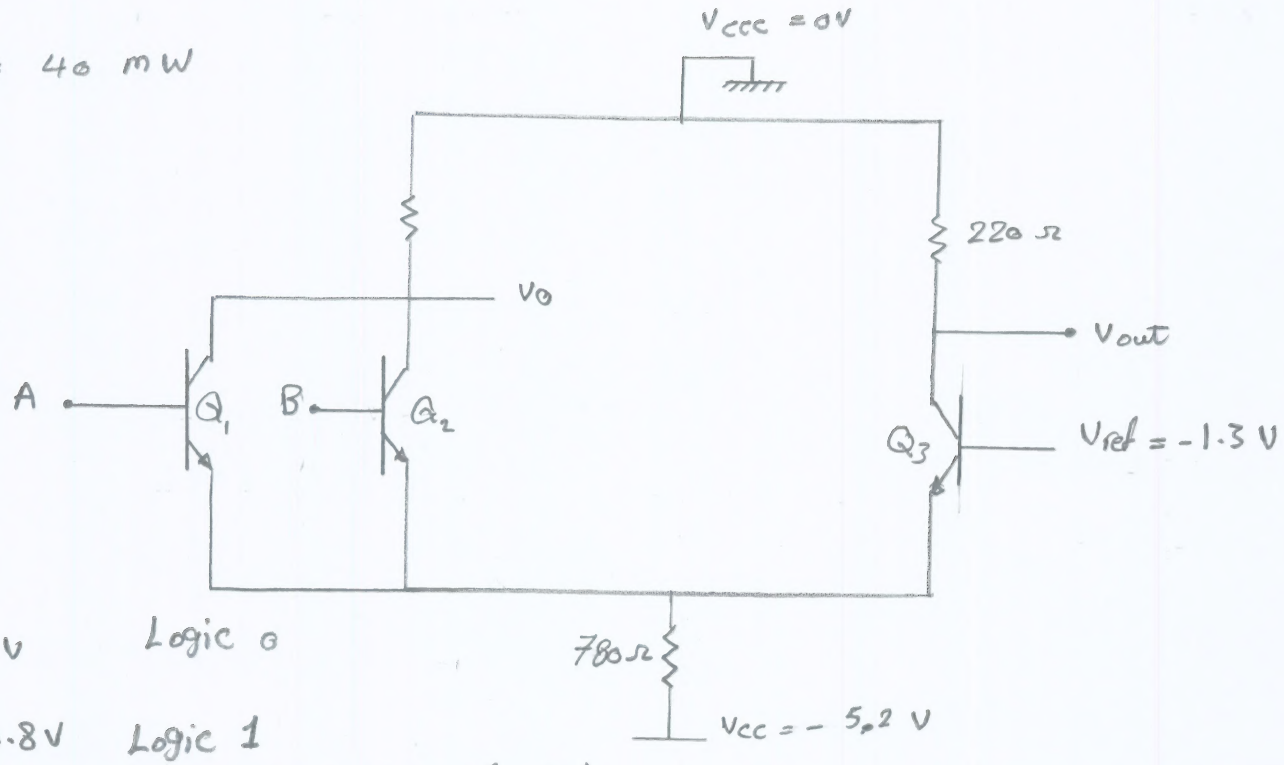
$T_{pd} < \ln 5 \simeq 0.8$ ns

* very fast than T.T.L
* Power supply (-)

- Hard to interface
- used in main Frame Coupler

$P_d = 40$ mW

Lower diss



$V_o \leq -1.7$ V Logic 0

$V_o \geq -0.8$ V Logic 1

(OR / NOR gate for ECL)

A, B (Low state ≤ -1.7 V)

at

$-1.3 > -1.7$

$V_B > V_E$

$Q \rightarrow$ on

$Q_3 \rightarrow$ on

$Q_1, Q_2 \rightarrow$ off

Conduction $\rightarrow$ Logic 0

A, B (High state ≥ -0.8 V)

$-0.8 > -1.3$

$V_E > V_B$

$Q_1, Q_2 \rightarrow$ on

$Q_3 \rightarrow$ off

output

(Q_1, Q_2) Low — Logic 0

(Q_3) Low — Logic 1